REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. Applicants would also like to thank the Examiner for correctly indicating as allowable the subject matter of dependent Claims 13, 23 and 32. This is in addition to dependent Claims 18, 27 and 36 that were previously indicated as having allowable subject matter. The arguments supporting patentability of the claims are provided below.

I. The Claimed Invention

The present invention, as recited in independent device Claim 10, for example, is directed to a dynamically reconfigurable processing unit comprising a microprocessor, and an embedded Flash memory for non-volatile storage of code, data and bit-streams. The embedded Flash memory comprises a field programmable gate array (FPGA) port. The dynamically reconfigurable processing unit further comprises a direct memory access (DMA) channel, and an S-RAM embedded FPGA for FPGA reconfigurations. The S-RAM embedded FPGA comprises an FPGA programming interface connected to the FPGA port of the embedded Flash memory through the DMA channel. The microprocessor, the embedded Flash memory, the DMA channel and the S-RAM embedded FPGA are integrated as a single chip.

The embedded S-RAM FPGA can thus be reconfigured so that the processing unit is dynamically reconfigurable. The dynamically reconfigurable processing unit advantageously supports application-dependent configurations. The embedded

Flash memory advantageously provides bit-streams from its FPGA port to the FPGA programming interface via the DMA channel so that the S-RAM embedded FPGA can be reconfigured. The DMA channel advantageously speed-ups downloading of the bit-streams to the FPGA programming interface.

Independent device Claim 19 is also directed to a reconfigurable processing unit comprising a microprocessor, a system bus connected to the microprocessor, and an embedded Flash memory comprising a code port and a data port connected to the system bus for interfacing with the microprocessor. The Flash memory also comprises a field programmable gate array (FPGA) port. A direct memory access (DMA) channel is connected to the system bus and to the FPGA port of the embedded Flash memory. An embedded FPGA is for FPGA reconfigurations and comprises a FPGA programming interface connected to the DMA channel for interfacing with the FPGA port of the Flash memory.

Independent method Claim 28 is directed to a method for making a reconfigurable processing unit as defined in independent device Claim 10.

II. The Claims Are Patentable

Independent Claim 10 was rejected over the Bocchi patent in view of the IEEE article by Brown et al. and in further view of the Iwata et al. patent. Independent Claims 19 and 28 were rejected over the Bocchi patent in view of the Brown et al. article.

The Examiner cited the Bocchi patent as disclosing in FIG. 1 a processing unit 10 comprising a microprocessor 66; an

embedded Flash memory 62 for non-volatile storage of code, data and bit-streams, wherein the embedded Flash memory comprises a field programmable gate array (FPGA) port; and a direct memory access (DMA) channel between the Flash memory 62 and the FPGA 64 or the SRAM 68 via the CPLD 60. The DMA channel is connected to the FPGA 64 and the SRAM 68 and comprises a CPLD 60 interface connected to an FPGA port and to a port of the Flash memory 62.

As correctly noted by the Examiner, the Bocchi patent does not disclose that the FPGA 64 is an SRAM embedded FPGA. The Examiner cited Brown et al. as disclosing an SRAM associated with a FPGA (TABLE 1 on page 45, and page 53, column 1). As also correctly noted by the Examiner, the Bocchi patent does not disclose that the microprocessor 66, the Flash memory 62, and the FPGA 64 are all integrated on a single chip. The Examiner cited Iwata et al. as disclosing in FIG. 1 a microprocessor 3, a Flash memory 5, and an SRAM 6 all integrated on a single chip.

The Examiner has taken the position that it would have been obvious to one of skill in the art at the time of the invention to 1) incorporate the teachings of Bocchi and Brown et al. (i.e., utilize an SRAM for the FPGA); and 2) incorporate the teachings of Bocchi and Iwata et al. (i.e., place the microprocessor, the SRAM and the Flash memory on the same chip to reduce system size and cost.)

The Applicants submit that one of ordinary skill in the art would not seek to selectively modify Bocchi in view of Brown et al. and in further view of Iwata et al. in an attempt to produce the claimed invention. This is especially so since

Bocchi fails to disclose that the FPGA 64 is to be reconfigurable.

In the Bocchi patent, the CPLD 60 (which is characterized as the DMA) is a blank controller programmed with interface functions (FIG. 3 in Bocchi) through an IEEE Standard 1149.1 (JTAG) port. Upon power-on or reset, the interface functions of the CPLD 60 cause it to decode and coordinate access to the functionality of the other components of the processor card 14. The CPLD 60 provides interface functions for the Flash memory 62, the FPGA 64 and the microprocessor 64. The interface provided by the CPLD 60 still functions in case the microprocessor 66 fails.

The CPLD 60 is used to provide application data to the FPGA 64 from the Flash memory 62. The application data is not used to reconfigure the FPGA 64 as in the claimed innvetion. Reference is directed to column 5, lines 5-14 of Bocchi, which provides:

> "For the controller 10 to function correctly after power-on or reset, additional steps must be completed after programming the CPLD 60. Valid programs must be downloaded from the application program into the flash memory 62. Code for the field-programmable gate array (FPGA) 64 and the embedded code for the central processing unit (CPU) 66 is downloaded into the flash memory 62 through a flash programming port (not shown), which is a parallel interface to the CPLD 60." (Emphasis added).

Reference is also directed to column 5, lines 22-27 of Bocchi, which provides:

> "The code for the FPGA 64 is loaded from the flash memory 62, programming the FPGA 64 with certain logic functions, shown in FIGS. 4-9 and to be discussed hereinafter. After the code for the FPGA 64 is loaded, the controller 10 will begin operating in accordance with the embedded code of the CPU 66, shown in FIGS. 10-17."

Even though the FPGA 64 in Bocchi receives application data from the Flash memory 62 via the CPLD 60, it is not for reconfiguring the FPGA 64. While the Brown et al. article discloses an SRAM associated with a FPGA, one of skill in the art would not be motivated to selectively incorporate such a device into a controller 10 as disclosed in Bocchi so that an S-RAM embedded FPGA is to be reconfigured. The Iwata et al. patent also fails to teach or suggest modifying the Bocchi patent for replacing the FPGA 64 with an S-RAM embedded FPGA that is to be reconfigured.

It appears that the Examiner is using impermissible hindsight reconstruction to modify Bocchi in view Brown et al. and in further view of Iwata et al. The prior art references, individually or in combination, do not teach or suggest the claimed invention.

Accordingly, it is submitted that independent Claim 10 is patentable over Bocchi in view Brown et al. and in further view of Iwata et al. Independent Claims 19 and 28 are similar to

Independent Claim 10. Therefore, it is submitted that these claims are also patentable over Bocchi in view Brown et al. and in further view of Iwata et al.

In view of the patentability of independent Claims 10, 19 and 28, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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